

# PH6325L

N-channel TrenchMOS™ logic level FET

Rev. 01 — 28 April 2004

Preliminary data

## 1. Product profile

### 1.1 Description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Optimized for use in DC-to-DC converters
- Low threshold voltage
- Very low switching and conduction losses
- Low thermal resistance.

### 1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- Notebook computers.

### 1.4 Quick reference data

- $V_{DS} \leq 25$  V
- $I_D \leq 78.7$  A
- $Q_{gd} = 3.3$  nC (typ)
- $Q_{g(tot)} = 13.3$  nC (typ)
- $R_{DSon} \leq 6.3$  m $\Omega$  ( $V_{GS} = 10$  V)
- $R_{DSon} \leq 9.5$  m $\Omega$  ( $V_{GS} = 4.5$  V).

## 2. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBL286</p> <p><b>SOT669 (LFAK)</b></p>	<p>MBB076</p>
4	gate (g)		
mb	mounting base; connected to drain (d)		



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### 3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PH6325L	LFPAK	Plastic single-ended surface mounting package; 4 leads	SOT669

### 4. Limiting values

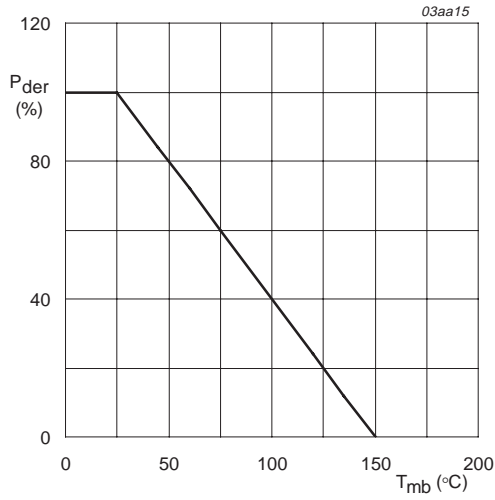
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	25	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Figure 2 and 3</a>	-	78.7	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Figure 2</a>	-	49.6	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ <a href="#">Figure 3</a>	-	236	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Figure 1</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	208	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 34\text{ A};$ $t_p = 0.15\text{ ms}; V_{DD} = 25\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V};$ starting at $T_j = 25\text{ °C}$	-	115	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 3.4\text{ A};$ $t_p = 0.015\text{ ms}; V_{DD} = 25\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V};$ starting at $T_j = 25\text{ °C}$	[1] - [2]	1.2	mJ

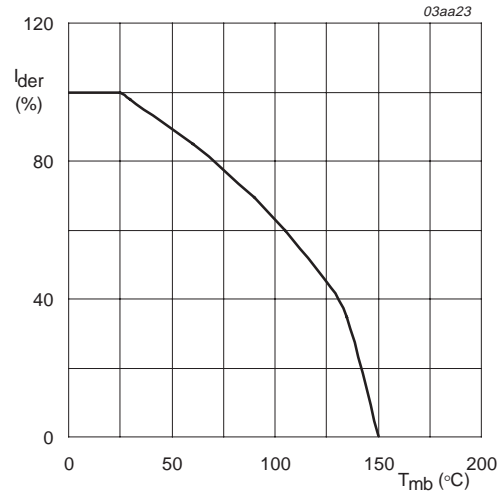
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



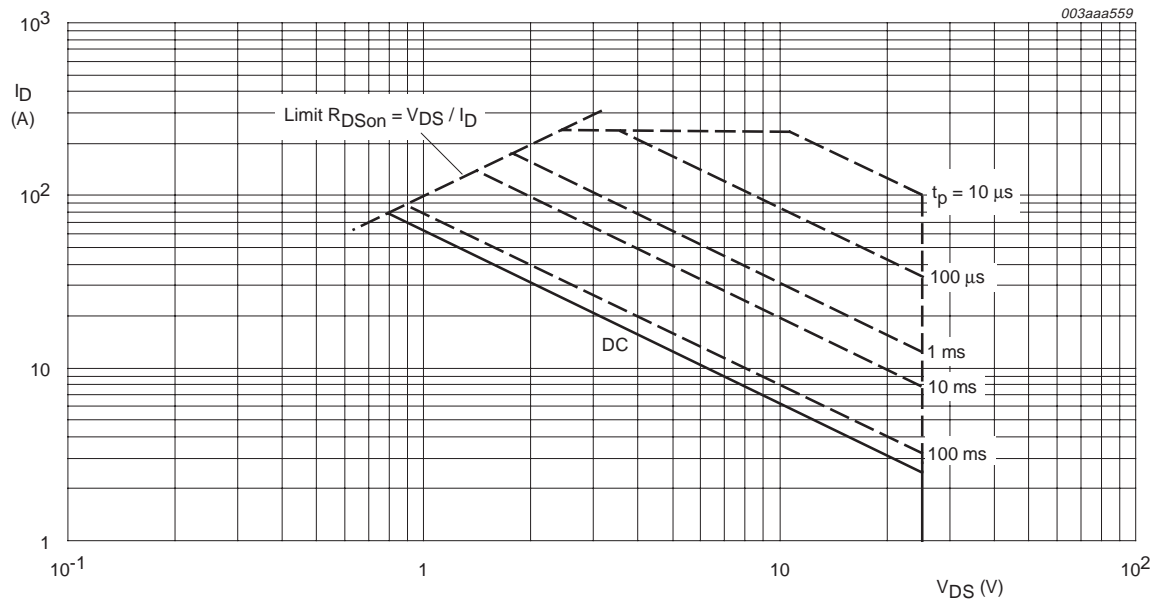
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

### 5.1 Transient thermal impedance

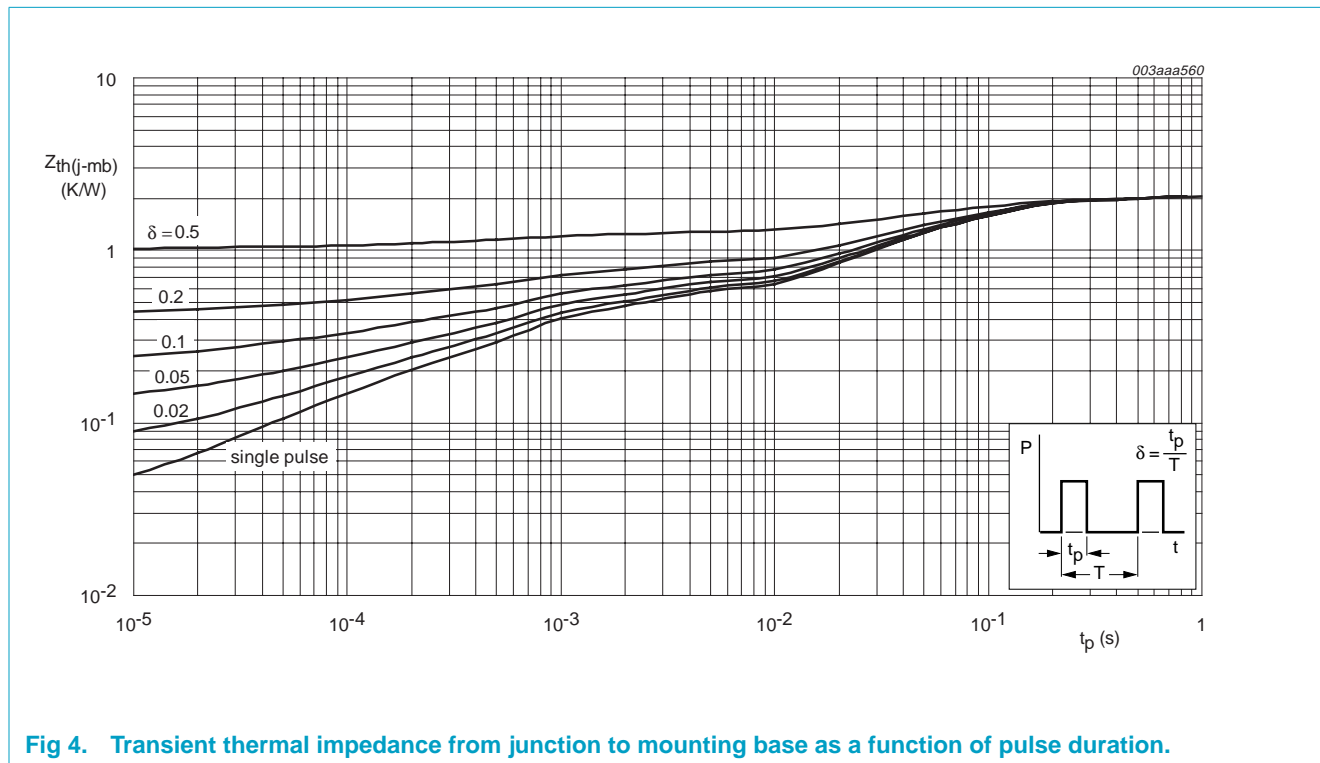


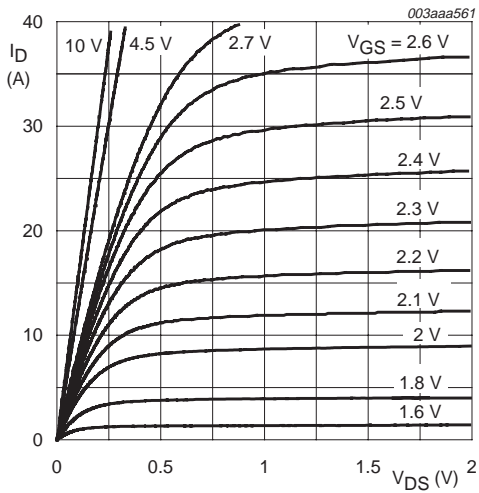
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 6. Characteristics

**Table 5: Characteristics**

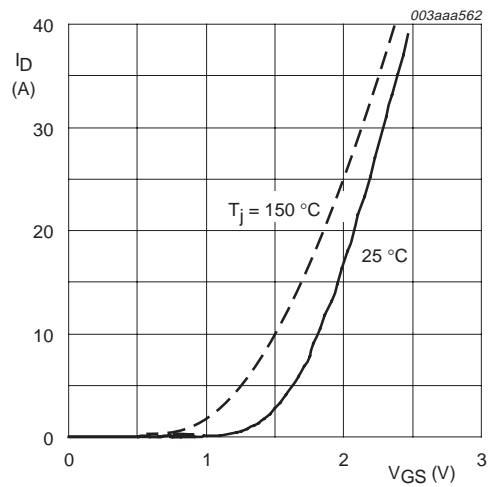
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; <b>Figure 9 and 10</b>				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.5	-	-	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 25\text{ V}$ ; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.06	1	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 16\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; <b>Figure 7 and 8</b>				
		$T_j = 25\text{ °C}$	-	7.4	9.5	m $\Omega$
		$T_j = 150\text{ °C}$	-	11.8	15.2	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; <b>Figure 7 and 8</b>				
		$T_j = 25\text{ °C}$	-	4.7	6.3	m $\Omega$
		$T_j = 150\text{ °C}$	-	7.5	10.1	m $\Omega$
$R_{G(int)}$	internal gate resistance	$f = 1\text{ MHz}$	-	1.8	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <b>Figure 11 and 12</b>	-	13.3	-	nC
$Q_{gs}$	gate-source charge		-	4.9	-	nC
$Q_{gs1}$	pre- $V_{GS(th)}$ gate-source charge		-	2.6	-	nC
$Q_{gs2}$	post- $V_{GS(th)}$ gate-source charge		-	2.3	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	3.3	-	nC
$V_{plat}$	plateau voltage		-	2.4	-	V
$Q_{g(tot)}$	total gate charge	$I_D = 0\text{ A}$ ; $V_{DS} = 0\text{ V}$ ; $V_{GS} = 4.5\text{ V}$	-	11.1	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 12\text{ V}$ ; $f = 1\text{ MHz}$ ; <b>Figure 13 and 14</b>	-	1871	-	pF
$C_{oss}$	output capacitance		-	517	-	pF
$C_{rss}$	reverse transfer capacitance		-	179	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $f = 1\text{ MHz}$	-	2420	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{GS} = 4.5\text{ V}$ ; $R_G = 4.7\text{ }\Omega$	-	25	-	ns
$t_r$	rise time		-	25	-	ns
$t_{d(off)}$	turn-off delay time		-	32	-	ns
$t_f$	fall time		-	12	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; <b>Figure 15</b>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	33	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_R = 25\text{ V}$	-	13	-	nC



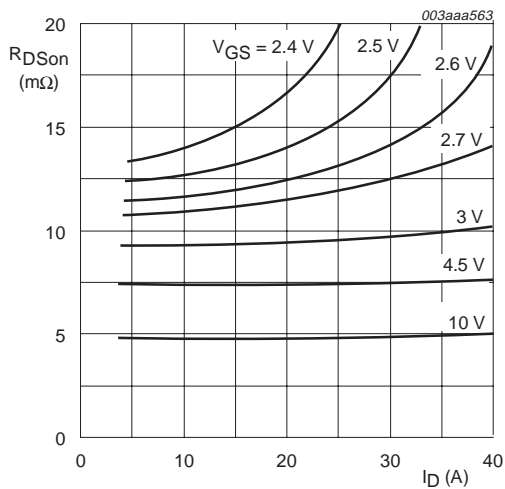
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



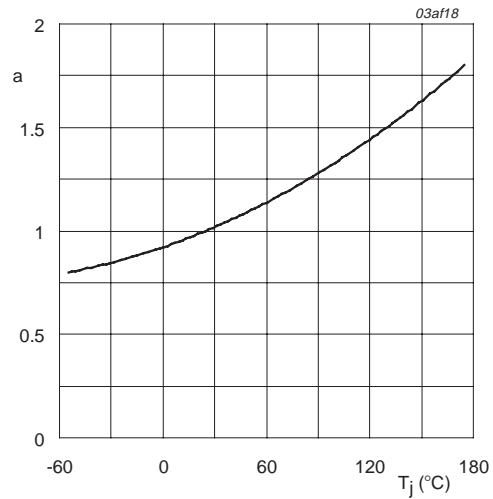
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



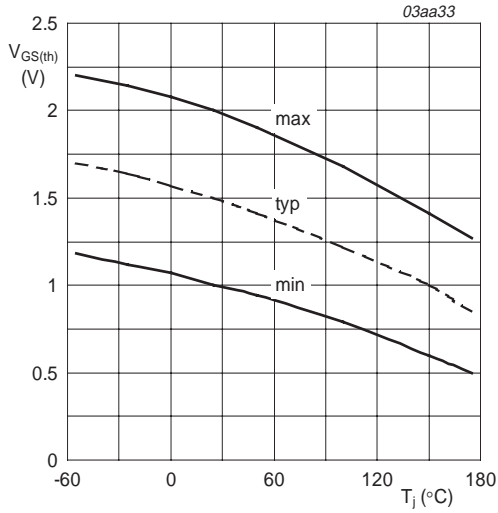
$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



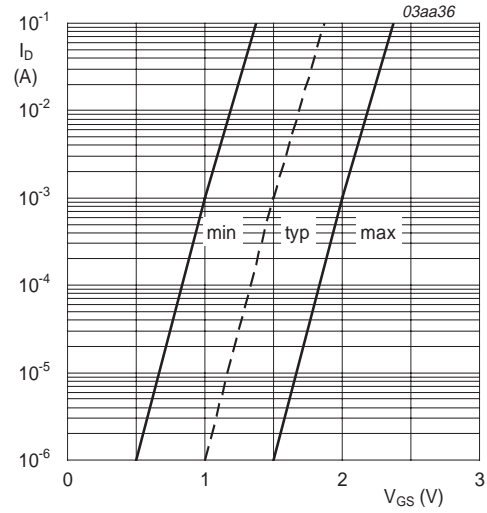
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



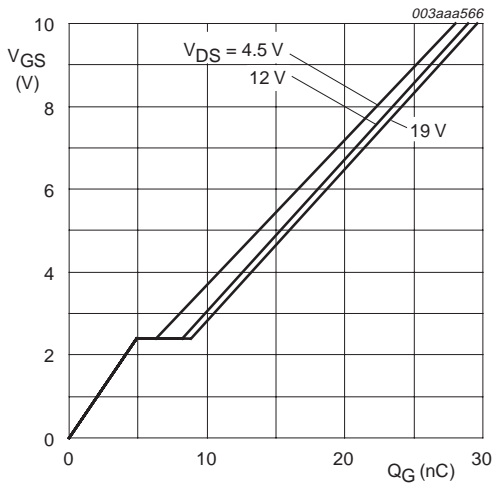
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$I_D = 25 \text{ A}; V_{DS} = 4.5 \text{ V}, 12 \text{ V and } 19 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values.

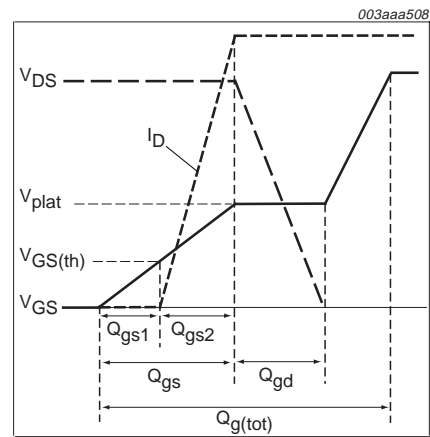
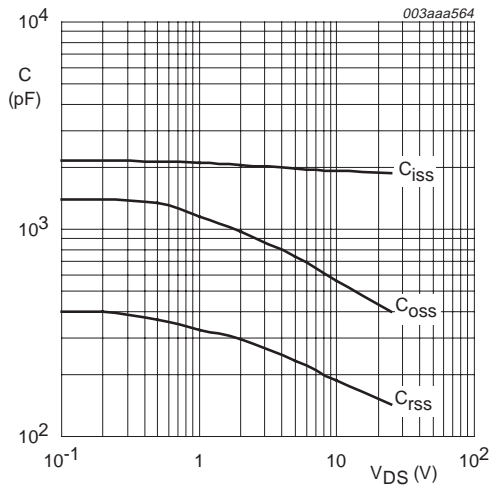
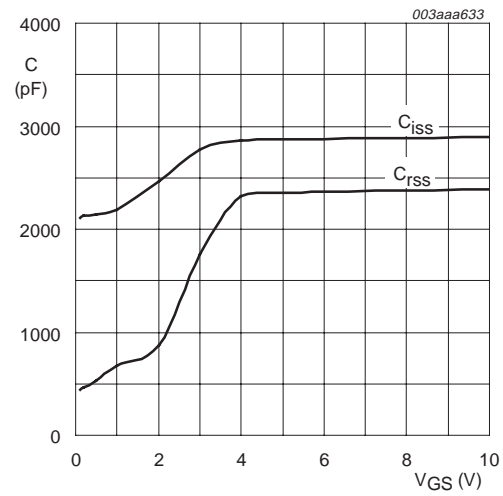


Fig 12. Gate charge waveform definitions.



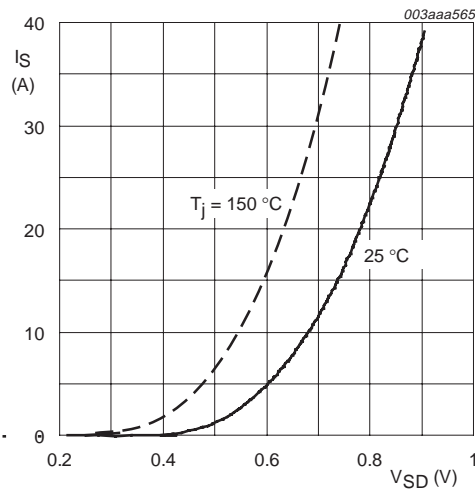
V<sub>GS</sub> = 0 V; f = 1 MHz

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



T<sub>j</sub> = 25 °C and 150 °C; V<sub>DS</sub> = 0 V

**Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values.**



T<sub>j</sub> = 25 °C and 150 °C; V<sub>GS</sub> = 0 V

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



7. Package outline

Plastic single-ended surface mounted package (Philips version LFPACK); 4 leads

SOT669

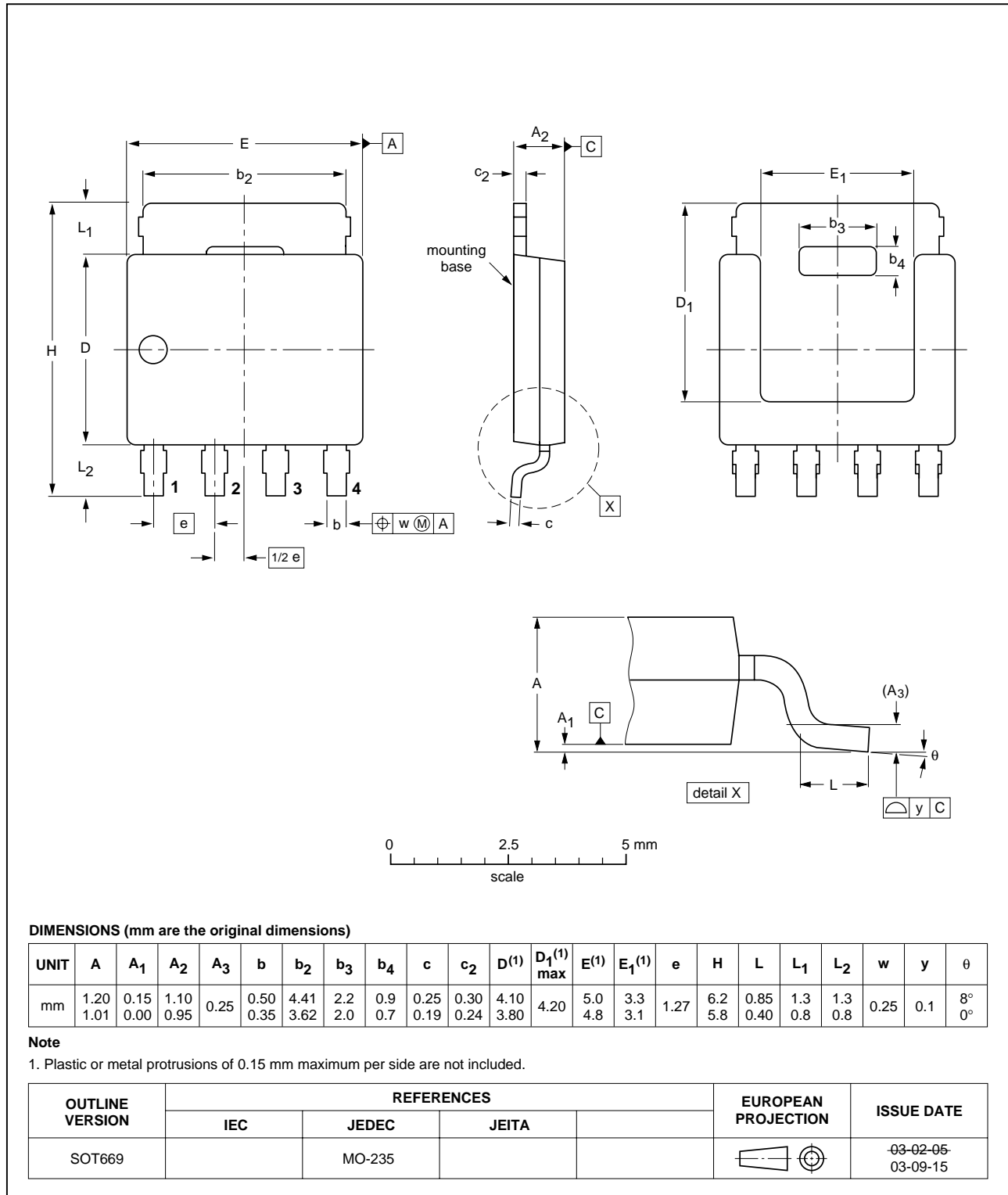


Fig 16. SOT669 (LFPACK).

8. Soldering

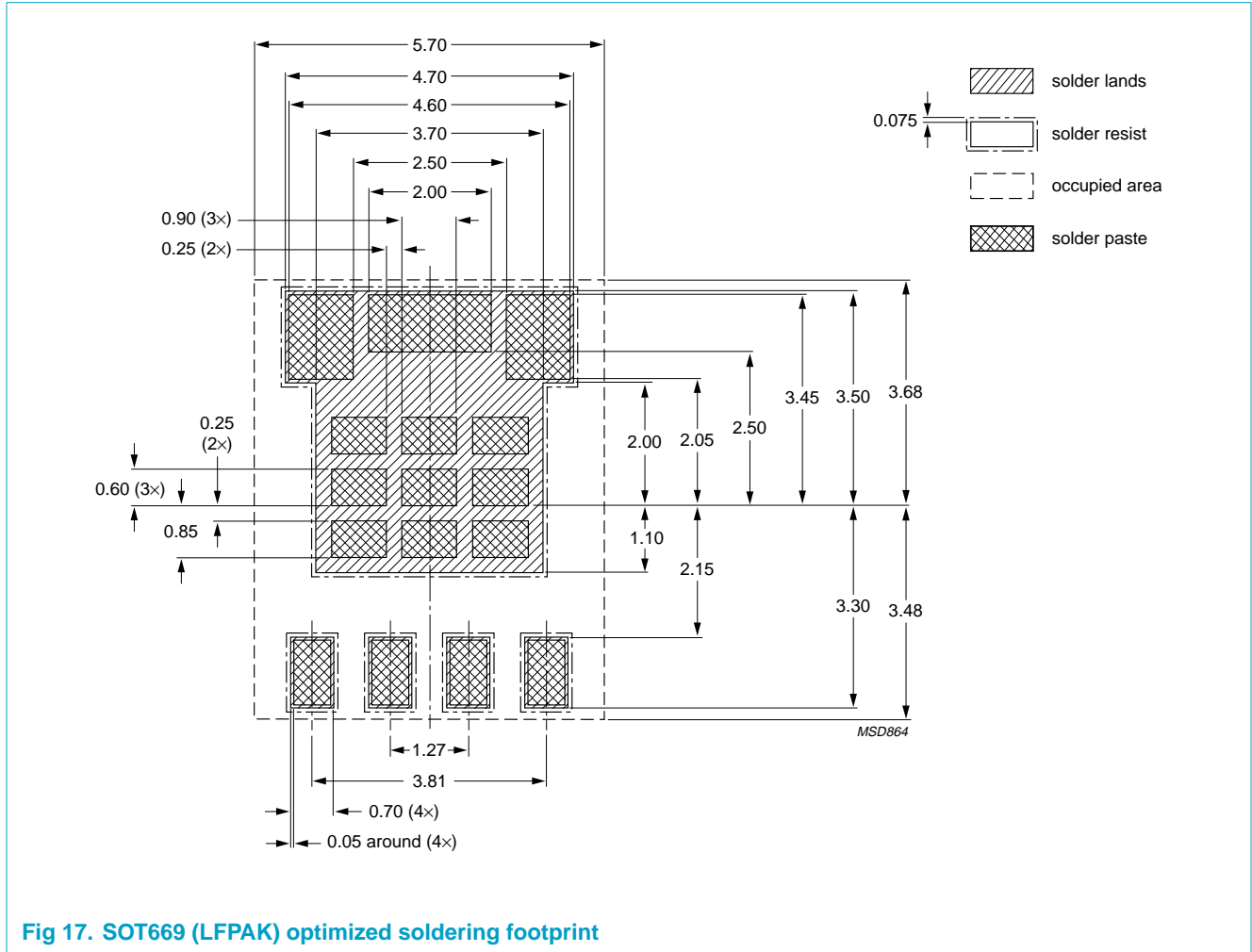


Fig 17. SOT669 (LFPAK) optimized soldering footprint

## 9. Revision history

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Table 6: Revision history

Rev	Date	CPCN	Description
01	20040428	-	Preliminary data (9397 750 12307)

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## 10. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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